

**6E7104**

Roll No. \_\_\_\_\_

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**6E7104**

**B.Tech. VI Sem. (Main) Examination, July- 2023**  
**Computer Science and Engg.)**  
**6CS4-04 : Computer Architecture and Organization**  
**CS,IT,AID,CAI**

Time : 3 Hours

Maximum Marks : 70

**Instructions to Candidates:**

Attempt all Ten questions from Part A, Five question out of Seven from Part B and Three questions out of Five Questions from Part C.

Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used/ calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No.205).

**PART - A**

Answer should be given up to 25 words only.

All questions are compulsory.

(10×2=20)

1. ✓ Is there any difference between microprocessor and microcontroller? Explain with example.
2. ✓ Define (r-1)'s complement and r's complement using an example.
3. ✓ Distinguish among computer organization and computer architecture.
4. ✓ Explain RISC.
5. ✓ Explain the use of cache memory.
6. ✓ What are the different conflicts that will arise in pipeline? How do you remove the conflicts? Describe.
7. ✓ Describe subroutine.
8. ✓ Draw and explain the memory hierarchy in a digital computer.
9. ✓ Perform the 2's complement subtraction of smaller number (101011) from largernumber (111001).
10. ✓ What are the basic difference among a branch instruction, a call subroutine instruction and program interrupt?

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(1)

[Contd....]

111001  
010101  
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1001110

2142

PART - B

Analytical/Problem solving questions.

Attempt any Five questions.

(5×4=20)

1. Explain the Fetch Cycle with diagram.
2. Multiply  $(-37) \times (21)$  using Booth multiplier algorithm and write all the steps.
3. Describe the Flynn model and explain the components.
4. Write short note on:
  - 1) Memory address register
  - 2) Program Counter
5. Explain paging and segmentation with the help of suitable example.
6. Describe the procedure for addition and subtraction for fixed-point number? Explain it by use of Flowchart.
7. Explain how virtual address is translated into real address in segmented memory system.

PART - C

Descriptive/Analytical/Problem Solving/Design questions.

Attempt any Four questions.

(3×10=30)

1. Describe role of addressing modes used in computer architecture. Illustrate direct and indirect addressing mode with suitable example. Demonstrate arithmetic micro operation and draw diagram of 4-bit full adder.
2. a) Explain arithmetic pipeline with a suitable example. Draw diagram also. [4]  
b) Discuss all factor which affect the performance of pipelining processor based systems. A non-pipeline system takes 100 ns to process a task. The same task can be processed in a six-segment pipeline with a clock cycle of 20ns. Determine the speedup ratio of the pipeline for 200 tasks. What is maximum speedup that can be achieved? [3+3]
3. a) Explain cache coherency and why it's necessary? Explain Different approaches for cache coherency. [6]  
b) Construct a memory system having static 1K x 4 RAM. How many such RAMs required to  
i) Construct 1K x RAM memory bank and 4K x 4RAM memory bank. [4]
4. Differentiate between Hardwired control unit and Micro-Programmed Control unit with their diagram.
5. a) Draw and explain the diagram of a DMA controller. Why read write lines of DMA are Bidirectional. [5+1]  
b) What is the function IOP? Explain it with block Diagram. [4]

0011110101  
+1  
0011110110